Amendments to the Claims

Claim 1 to 18. (canceled)

19. (currently amended) A resistance load source follower circuit comprising

(A) a transistor on a substrate, having a body connected to a body terminal, a gate connected to a gate terminal, a source connected to a source terminal, and a drain connected to a drain terminal, where there is no connection from a body terminal to a source terminal or from a body terminal to a drain terminal;

(B) a connection from said gate terminal to an input terminal;

(C) a resistance load having a first terminal and a second terminal;

(D) a connection from said source terminal and from said first terminal to an output terminal;

(E) a power supply having two terminals;

(F) a connection from the drain terminal of said transistor to one terminal of said power supply and a connection from said second terminal to the other terminal of said power supply; and

(G) a connection from said body terminal to a back bias control circuit, where said back bias control circuit independently controls the threshold voltage of said transistor to reduce power usage by said circuit, and a connection from said back bias circuit to said output terminal, and there is no connection from said back bias control circuit to a drain terminal.

20. (currently amended) A resistance load source follower circuit according to Claim 19 wherein said transistor is an N-channel transistor.

21. (canceled)

22. (new) A resistance load source follower circuit according to Claim 19 wherein said transistor is a P-channel transistor.

23. (new) A resistance load source follower circuit according to Claim 19 wherein said substrate is an SOI.

24. (new) A resistance load source follower circuit according to Claim 19 wherein said substrate is single crystal silicon.

25. (new) A resistance load source follower circuit according to Claim 24 wherein said substrate is undoped.

26. (new) A resistance load source follower circuit according to Claim 19 wherein at least some of the signals to said input terminal are analog.

27. (new) A resistance load source follower circuit according to Claim 19 that includes a level voltage shift circuit for shifting the input voltage to said transistor.

28. (new) A resistance load source follower circuit according to Claim 19 wherein said back bias control circuit shifts the threshold voltage of said transistor to achieve linearity when said resistance load source follower circuit is in active mode.

29. (new) A resistance load source follower circuit according to Claim 19 wherein said back bias control circuit shifts the threshold voltage of said transistor to achieve an off-state when said resistance load source follower circuit is in standby mode.

30. (new) An LSI having thereon at least one resistance load source follower circuit according to Claim 19.

31. (new) An LSI according to Claim 30 wherein at least one resistance load source follower circuit functions as an output buffer.

32. (new) An LSI according to Claim 30 wherein at least one resistance load source follower circuit functions as a voltage regulator.

33. (new) A resistance load source follower circuit according to Claim 19 wherein said

back bias control circuit alternatively applies the voltages of Vss or Vcc to said body terminal.

34. (new) A resistance load source follower circuit comprising

(A) a P-channel transistor on a substrate, having a body connected to a body terminal, a gate connected to a gate terminal, a source connected to a source terminal, and a drain connected to a drain terminal, where there is no connection from a body terminal to a source terminal or from a body terminal to a drain terminal;

(B) a connection from said gate terminal to an input terminal;

(C) a resistance load having a first terminal and a second terminal;

(D) a connection from said source terminal and from said first terminal to an output terminal;

(E) a power supply having two terminals;

(F) a connection from the drain terminal of said transistor to one terminal of said power supply and a connection from said second terminal to the other terminal of said power supply; and

(G) a connection from said body terminal to a back bias control circuit, where said back bias control circuit independently controls the threshold voltage of said transistor to reduce power usage by said circuit, and a connection from said back bias circuit to said output terminal, and there is no connection from said back bias control circuit to a drain terminal.

35. (new) A resistance load source follower circuit according to Claim 34 wherein said substrate is an SOI.

36. (new) A resistance load source follower circuit according to Claim 34 wherein said substrate is single crystal silicon.

37. (new) A source follower circuit comprising

(A) an N-channel transistor on a substrate, having a body connected to a body terminal, a gate connected to a gate terminal, a source connected to a source terminal, and a drain connected to a drain terminal, where there is no connection from a body terminal to a source terminal or from a body terminal to a drain terminal;

(B) a connection from said gate terminal to an input terminal;

(C) a resistance load having a first terminal and a second terminal;

(D) a connection from said source terminal and from said first terminal to an output terminal;

(E) a power supply having two terminals;

(F) a connection from the drain terminal of said transistor to one terminal of said power supply and a connection from said second terminal to the other terminal of said power supply; and

(G) a connection from said body terminal to a back bias control circuit, where

said back bias control circuit independently controls the threshold voltage of said transistor to reduce power usage by said circuit, and a connection from said back bias circuit to said output terminal, and there is no connection from said back bias control circuit to a drain terminal.

38. (new) A resistance load source follower circuit according to Claim 37 wherein said substrate is an SOI.

39. (new) A resistance load source follower circuit according to Claim 37 wherein said substrate is single crystal silicon.